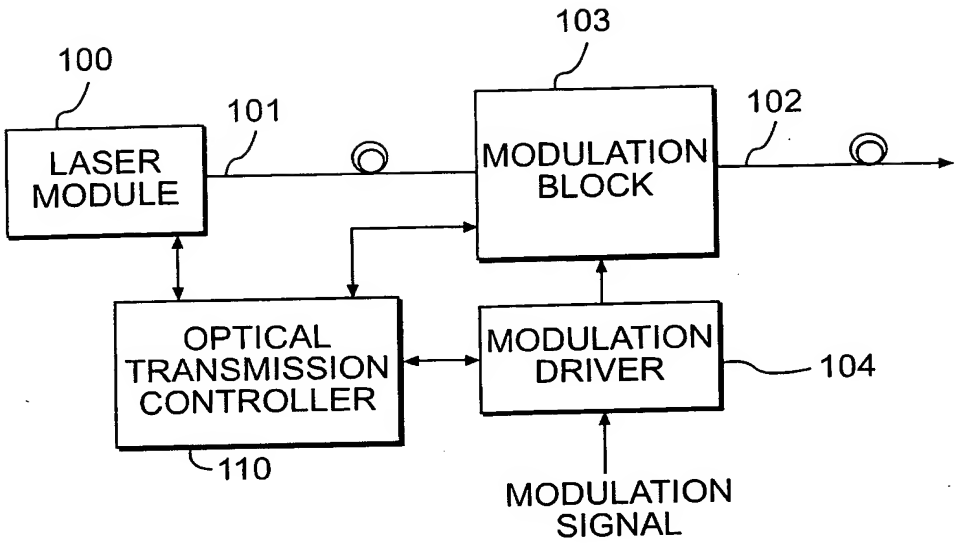


FIG. 1

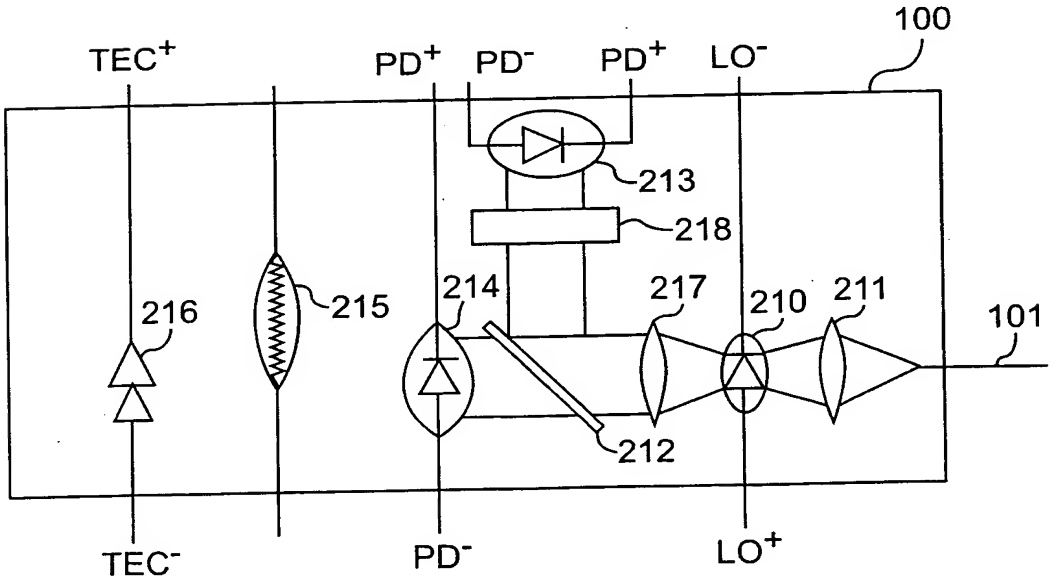
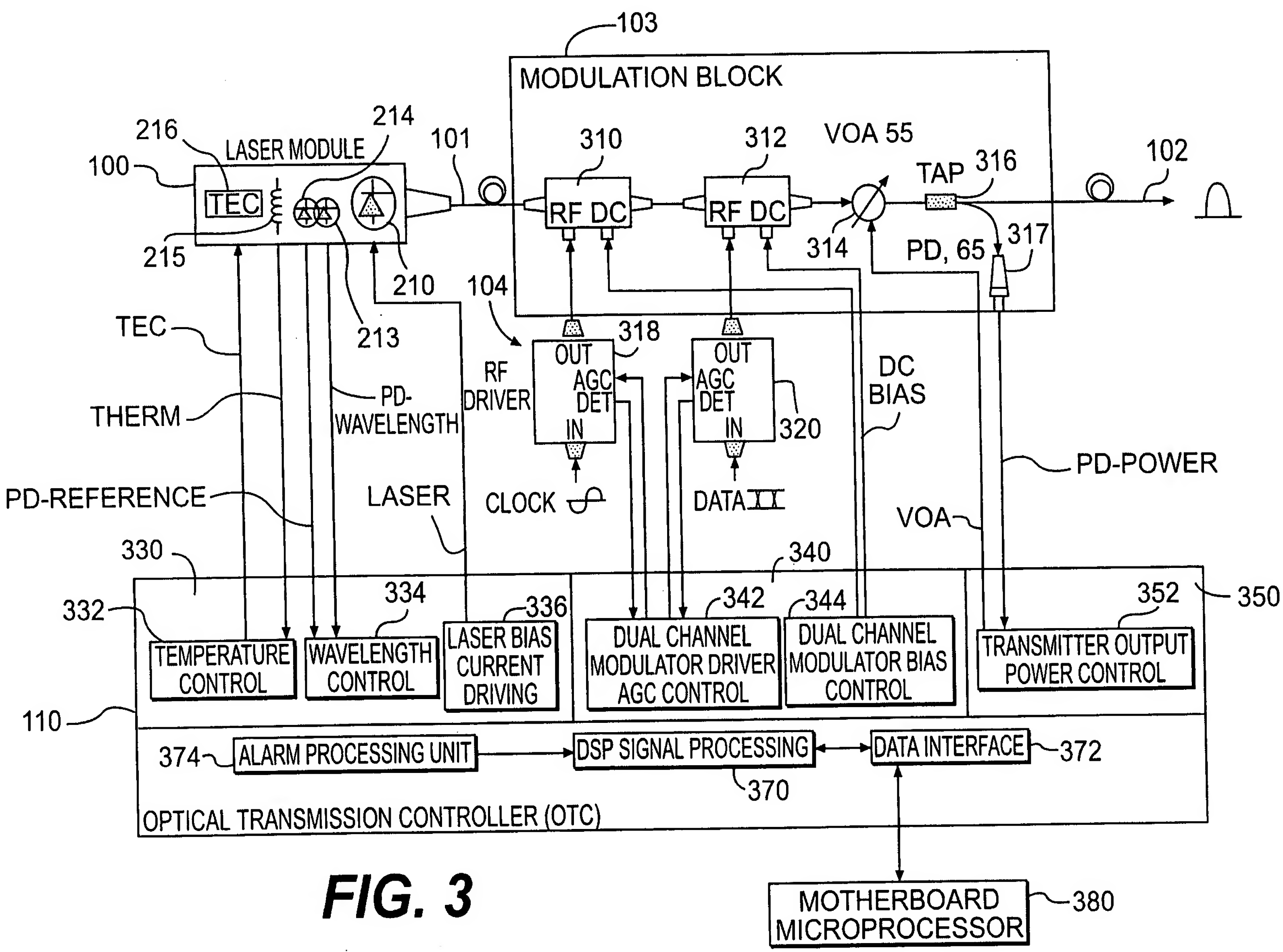


FIG. 2



MODULATION BLOCK
LASER MODULE
TEC
RF DC
RF DC
VOA 55
TAP
PD, 65
RF DRIVER
OUT
AGC
DET
IN
CLOCK
DATA
DC BIAS
PD-POWER
VOA
TEC
THERM
PD-WAVELENGTH
PD-REFERENCE
LASER
TEMPERATURE CONTROL
WAVELENGTH CONTROL
LASER BIAS CURRENT DRIVING
DUAL CHANNEL MODULATOR DRIVER AGC CONTROL
DUAL CHANNEL MODULATOR BIAS CONTROL
TRANSMITTER OUTPUT POWER CONTROL
ALARM PROCESSING UNIT
DSP SIGNAL PROCESSING
DATA INTERFACE
OPTICAL TRANSMISSION CONTROLLER (OTC)
MOTHERBOARD MICROPROCESSOR

FIG. 3

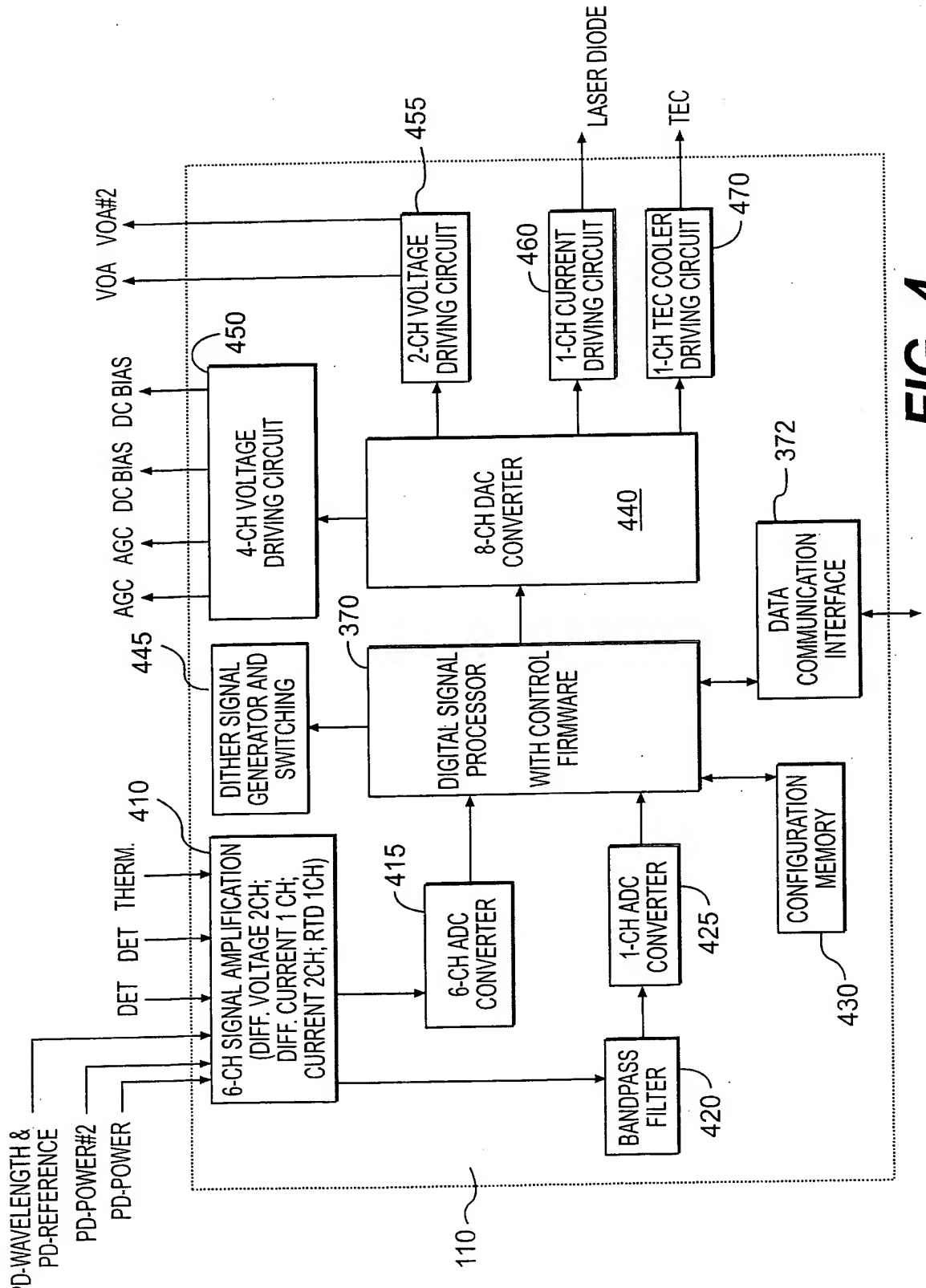

PD-WAVELENGTH & PD-REFERENCE
PD-POWER#2
PD-POWER
DET
DET
THERM.
410
6-CH SIGNAL AMPLIFICATION (DIFF. VOLTAGE 2CH; DIFF. CURRENT 1 CH; CURRENT 2CH; RTD 1CH)
415
6-CH ADC CONVERTER
BANDPASS FILTER
420
1-CH ADC CONVERTER
425
CONFIGURATION MEMORY
430
110
445
DITHER SIGNAL GENERATOR AND SWITCHING
370
DIGITAL SIGNAL PROCESSOR WITH CONTROL FIRMWARE
8-CH DAC CONVERTER
440
372
DATA COMMUNICATION INTERFACE
AGC
AGC
DC BIAS
DC BIAS
450
4-CH VOLTAGE DRIVING CIRCUIT
VOA
VOA#2
455
2-CH VOLTAGE DRIVING CIRCUIT
460
1-CH CURRENT DRIVING CIRCUIT
LASER DIODE
470
1-CH TEC COOLER DRIVING CIRCUIT
TEC

FIG. 4

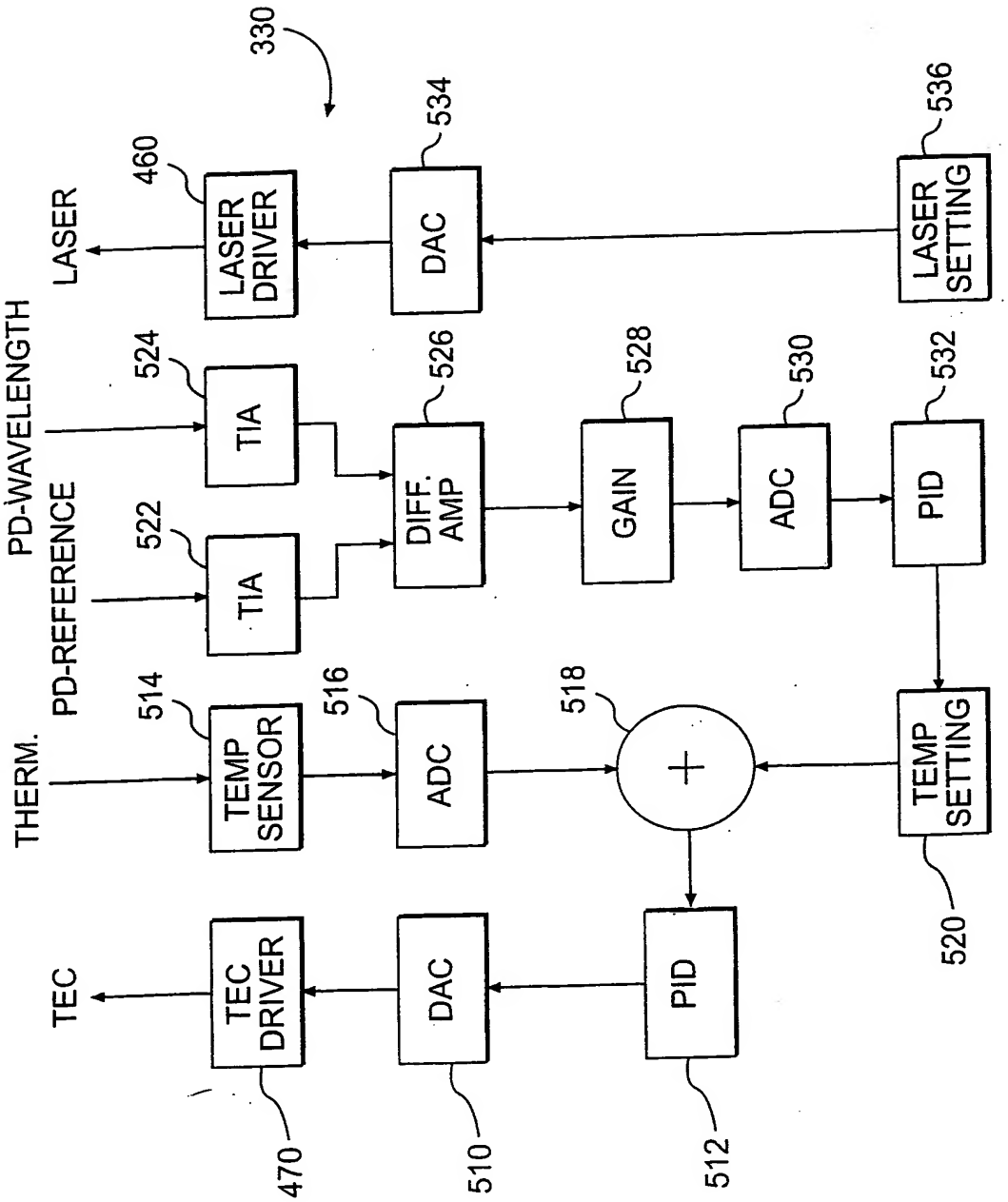

330
460
LASER DRIVER
LASER
534
DAC
536
LASER SETTING
524
TIA
PD-WAVELENGTH
526
DIFF. AMP
528
GAIN
530
ADC
532
PID
522
TIA
PD-REFERENCE
514
TEMP SENSOR
THERM.
516
ADC
518
+
TEMP SETTING
520
TEC
TEC DRIVER
DAC
PID
470
510
512

FIG. 5A

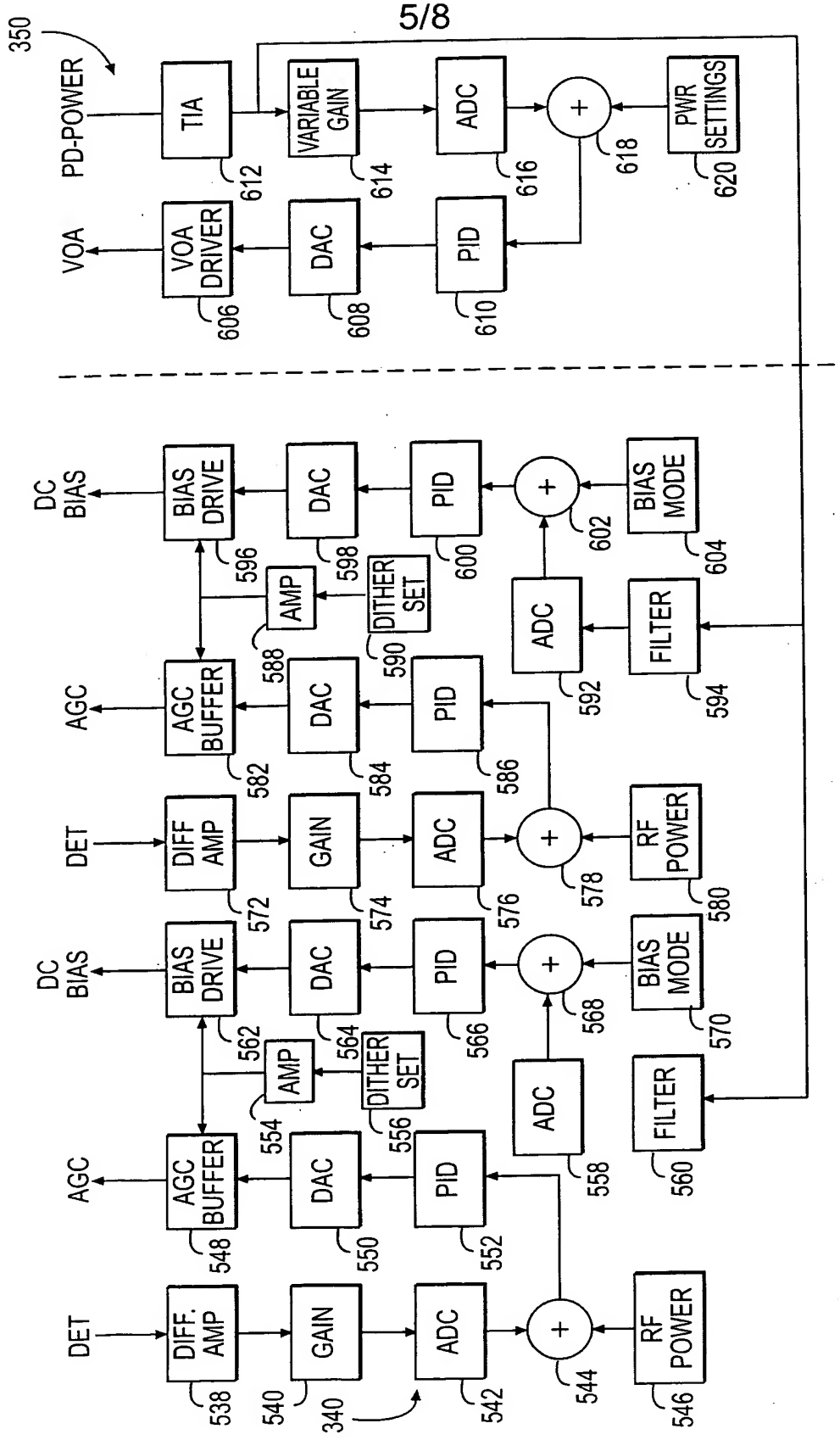

350
PD-POWER
TIA
612
VARIABLE GAIN
614
ADC
616
618
PWR SETTINGS
620
VOA
VOA DRIVER
606
DAC
608
PID
610
DC BIAS
BIAS DRIVE
596
DAC
598
PID
600
602
BIAS MODE
604
AMP
588
DITHER SET
590
ADC
592
FILTER
594
AGC
AGC BUFFER
582
DAC
584
PID
586
DET
DIFF AMP
572
GAIN
574
ADC
576
578
RF POWER
580
DC BIAS
BIAS DRIVE
562
DAC
564
PID
566
568
BIAS MODE
570
AMP
554
DITHER SET
556
ADC
558
FILTER
560
AGC
AGC BUFFER
548
DAC
550
PID
552
DET
DIFF. AMP
538
GAIN
540
340
ADC
542
544
RF POWER
546

FIG. 5B

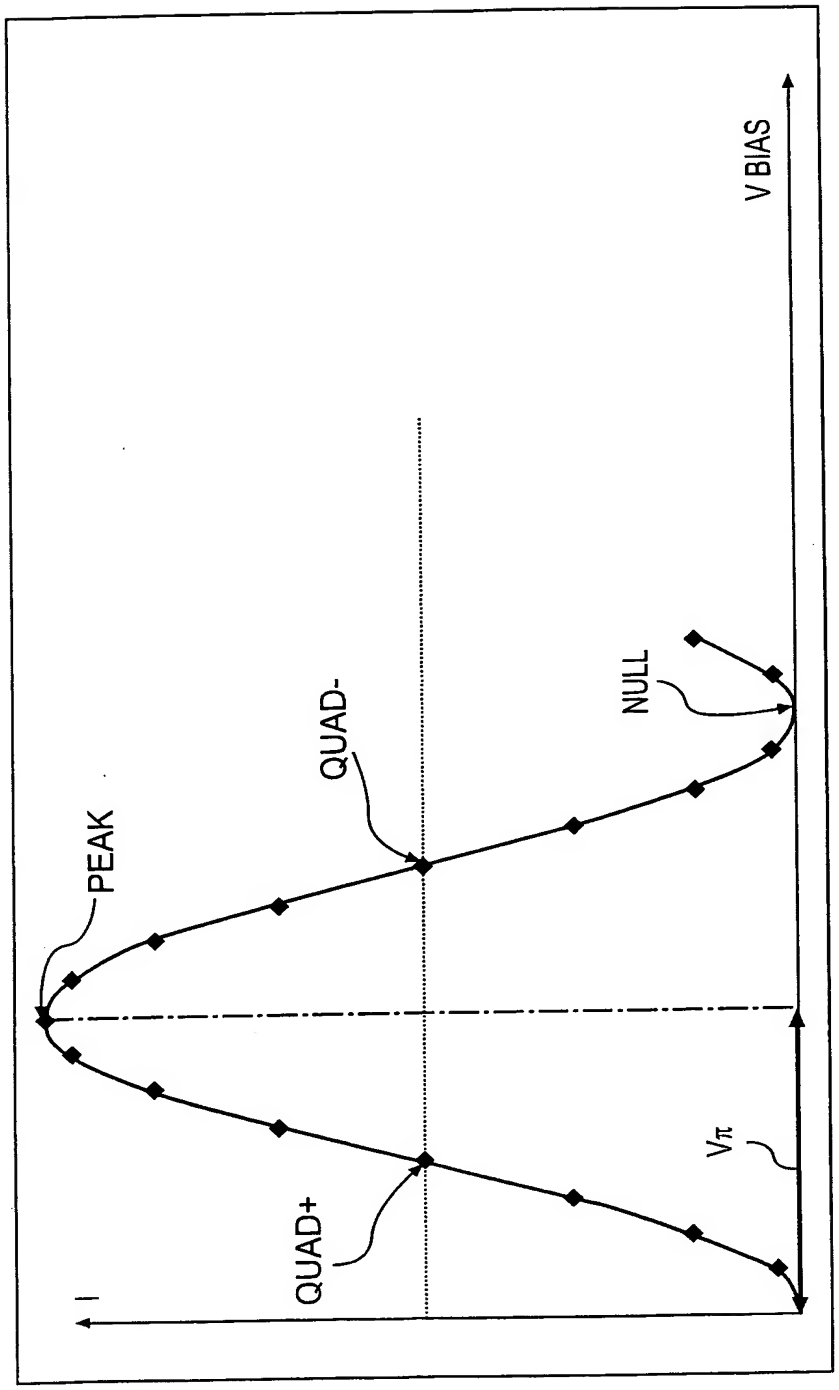


FIG. 6

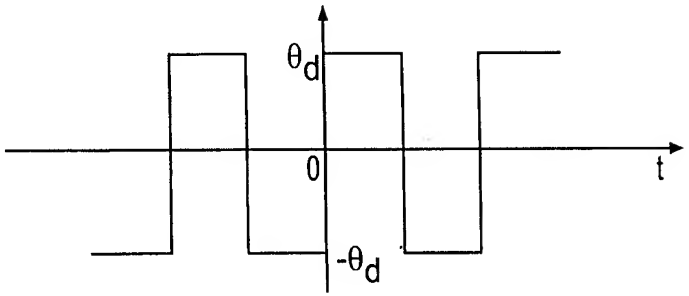


FIG. 7A

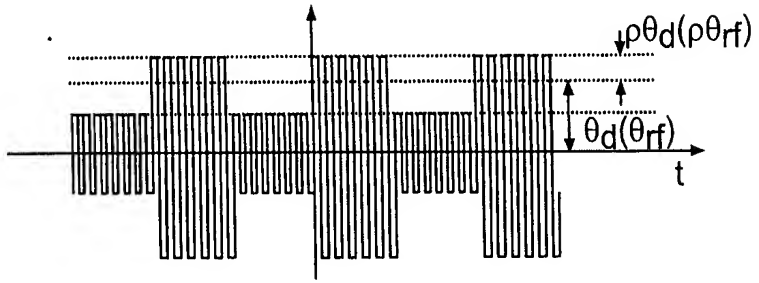


FIG. 7B

BIAS MODE	RF DRIVING	ERROR SIGNAL AMPLITUDE NORMALIZED TO P_m
GATED SQUARE DITHER TO DC PORT FOR QUAD+ CONTROL	SINUSOIDAL	$-2/\pi * \sin\theta_{dc} * \sin\theta_d * \sin(\rho\,\theta_d) * \text{BesselJ}(0,\theta_{rf})$
	SQUARE DIGITAL	$-2/\pi * \sin\theta_{dc} * \sin\theta_d * \sin(\rho\,\theta_d) * \cos\theta_{rf}$
SQUARE DITHER TO MODULATOR DRIVER FOR QUAD+ CONTROL	SINUSOIDAL	$-\rho/\pi * \sin\theta_{dc} * [1-\text{BesselJ}(0, 2\theta_{rf})]$
	SQUARE DIGITAL	$-2/\pi * \sin\theta_{dc} * \sin\theta_{rf} * \sin(\rho\,\theta_{rf})$
SQUARE DITHER TO DC PORT FOR PEAK CONTROL	SINUSOIDAL	$-2/\pi * \sin\theta_{dc} * \sin\theta_d * \text{BesselJ}(0,\theta_{rf})$
	SQUARE DIGITAL	$-2/\pi * \sin\theta_{dc} * \sin\theta_d * \cos\theta_{rf}$

FIG. 7C

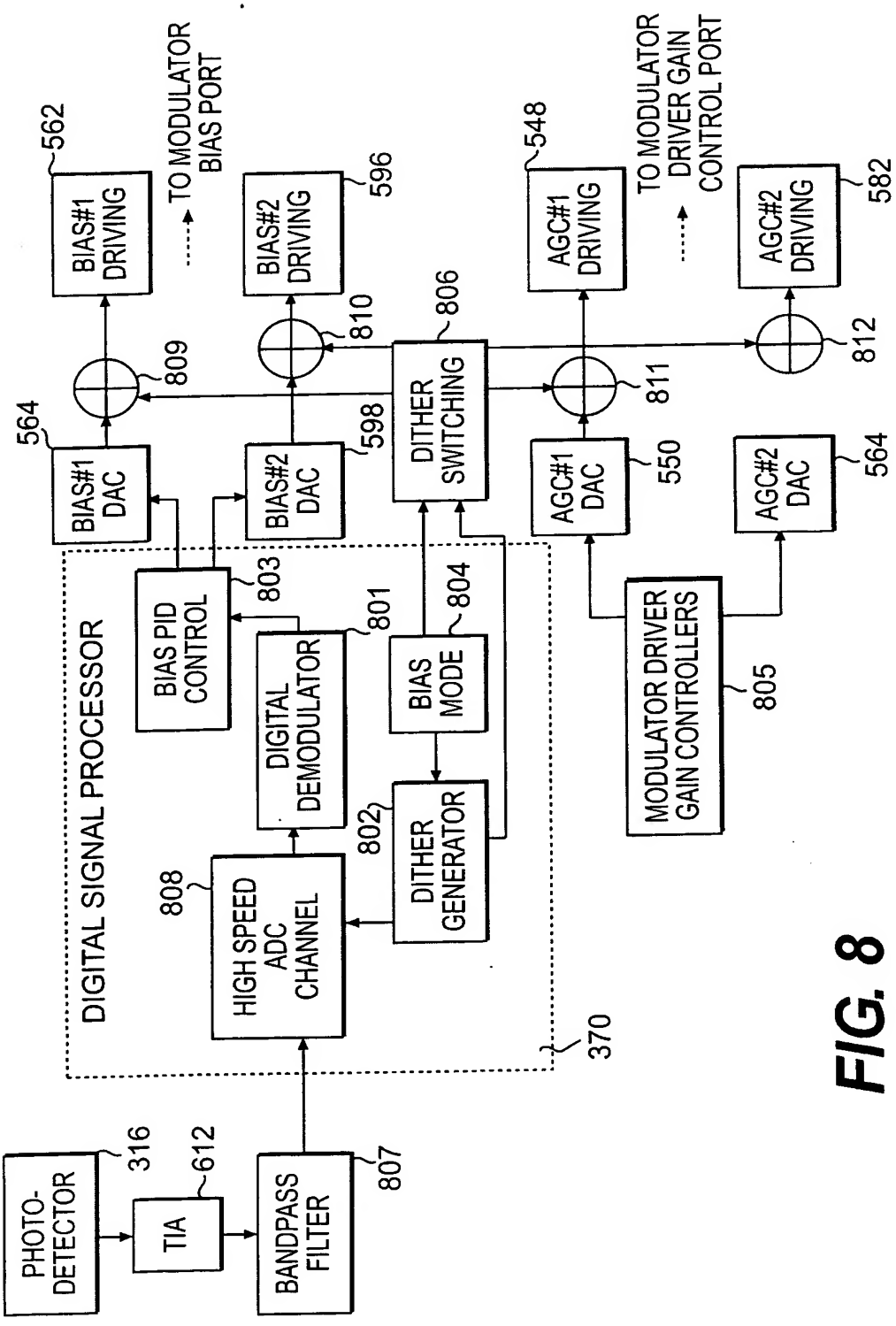


PHOTO-DETECTOR
316
TIA
612
BANDPASS FILTER
807
DIGITAL SIGNAL PROCESSOR
HIGH SPEED ADC CHANNEL
808
DIGITAL DEMODULATOR
801
BIAS PID CONTROL
803
DITHER GENERATOR
802
BIAS MODE
804
MODULATOR DRIVER GAIN CONTROLLERS
805
370
BIAS#1 DAC
564
BIAS#2 DAC
598
AGC#1 DAC
550
AGC#2 DAC
564
DITHER SWITCHING
806
809
810
811
812
BIAS#1 DRIVING
562
BIAS#2 DRIVING
596
AGC#1 DRIVING
548
AGC#2 DRIVING
582
TO MODULATOR BIAS PORT
TO MODULATOR DRIVER GAIN CONTROL PORT

FIG. 8